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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,740	08/05/2003	Hea-Suk Jung	51876P367	8831

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EXAMINER	
LE, THONG QUOC	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 08/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/635,740	JUNG, HEA-SUK	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☒ Claim(s) *3-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on 06/09/2005 has been entered.

2. Claims 8-14 have been canceled.

3. Claims 1-7 are presented for examination.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Response to Arguments

5. Applicant's arguments filed 06/09/2005 have been fully considered but they are not persuasive. Applicant's arguments is improper as described below:

> Kwon discloses a register controlled delay locked loop (DLL)that reduces current consumption by operating the DLL when a semiconductor device is only in an operation mode. Kwon discloses a clock divider 43 illustrated in Figure 4 does not generate a plurality of divided clock signals. That is, the clock divider disclosed by Kwon only generates one divided clock signal in response to a control signal based on CAS latency. Therefore, Kwon does not teach, disclose or suggest "...a clock divider to receive one of the internal clock signals and a control signal based on a column address strobe (CAS) signal to generate a plurality of divided signals, each having a predetermined pulse width adjusted by the control signal, and output a selected divided signal as the divided signal; and a DLL circuit to receive the plurality of internal clock signals and the divided signal to generate the delay locked clock signal."

Kwon disclosed a clock divider 13 in Figure 1 divides the rise_clk into n signals (n=8) and then produces a reference signal and divided clock signals div_in (Column 1, lines 43-47), and a divided clock signal is selected as the divided signal, "The clock divider 13

produces n clock signals in response to the second clock signal rise_clk, thereby forming the reference clock signal ref and the divided clock signal div_in (Column 2, lines 21-24).

synchronized with a rising edge of the clock signal clk. The clock divider **13** divides the second clock signal rise_clk into n signals (n: a positive integer, e.g., n=8) and then produces a reference signal ref and divided clock signals div_in.

produces the second clock signal rise_clk. The clock divider **13** produces n clock signals in response to the second clock signal rise_clk, thereby forming the reference clock signal ref and the divided clock signal div_in which are synchronized with the external clock signal clk every n divided clock signals.

As discussed above, the last action of final rejection is proper and stills stand.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting

directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1-2 are rejected under 35 U.S.C. 102(e) as being anticipated by Kwon et al. (U.S. Patent No. 6,768,690).

Regarding claim 1 Kwon et al. discloses a delay locked loop (DLL) block to generate a delay locked clock signal by delaying an external clock signal in a semiconductor device (Figure 4), comprising:

a clock buffer (41, 42) to receive the external clock signal (clk) and an inverted signal (/clk) of the external clock signal to generate a plurality of internal clock signals (fall_clk, rise_clk);

a clock divider (43, 55,56) to receive one of the internal clock signals (rise_clk) and a control signal (dll_en) based on a column address strobe (CAS) signal to generate a divided signal having a predetermined pulse (Figure 7, act_rasz) width adjusted by the control signal (Column 6, lines 21-29, Column 6, lines 5-29, 64-67, Column 7, lines 65-67, Column 8, lines 1-57); and

a DLL circuit (Figure 4, 40) to receive the plurality of internal clock signals (Column 1, lines 42-47) and the divided signal to generate the delay locked clock signal (Figure 4, ifclk, irclk).

Regarding claim 2, Kwon et al. disclose wherein the DLL circuit includes: a plurality of delay lines (Figure 4, 44,45, 46), each delay line having a plurality of unit delays, to delay the plurality of internal clock signals and the divided signal (Figure 4);

a delay model (Figure 4,52) to delay an output of the plurality of delay lines for a predetermined delay time to generate a feedback signal;

a phase comparator (Figure 4, 49) to compare a phase of a reference clock signal generated by the clock divider with a phase of the feedback signal in to generate a comparison signal, wherein the reference clock signal is an inverted version of the divided signal;

a shift controller (Figure 4, 48) to generate a shift right signal or a shift left signal according to the comparison signal; and

a shift register (Figure 4, 47) to adjust delay amount of the delay lines in response to the shift right signal or the shift left signal.

Allowable Subject Matter

8. Claims 3-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3-7 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Kwon et al. (U.S. Patent No. 6,768,690), and others, does not teach the claimed invention having a clock divider includes a first divider to receive the one of the internal clock signals to generate a first divided signal having a first pulse width and a first period; a second divider to receive the first divided signal in order to generate a second divided signal having the first pulse width and a second period and a third

divided signal having a second pulse width and the second period; a selector to selectively output the second divided signal and the third divided signal according to the control signal; a third clock divider to receive an output of the selector to generate the divided signal.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

THONG LE
PRIMARY EXAMINER